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EXAMINER
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ART UNIT	PAPER NUMBER
2826	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/865,704	ITO ET AL.	
	Examiner	Art Unit	
	Johannes P Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 March 2003 and 24 February 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14 and 29-63* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 29-63* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 03/21/2003 has been entered.

Response to Amendment

Amendment B filed 02/24/2003 has been entered in response to abovementioned Request for Continued Examination. In Amendment B Applicant substantially amended claims 1, 3, 34, 38 and 40. Comments on Remarks by Applicant contained in said Amendment B are included below under "Response to Arguments".

Response to Arguments

Remarks by Applicant as contained in Amendment B have been fully considered, but are not persuasive. In particular, Applicant states on page 7 that "Applicant is unable to construe FIG 3B as showing or suggesting a gentle peak in the p-type dopant distribution. Furthermore, there does not seem to be any gentle change in the depth direction of the impurity concentration depicted in FIG 3B". However, Prior Art Figure 3B

does show a gentle peak in the impurity concentration profile in the second conductivity type region because of the canceling effect of impurities of opposite polarity (As (n) and B(p)). Furthermore, judging from Figure 3B, the change in the depth direction of said impurity concentration appears to be as gentle as can be expected considering the usual experimental ripples included in said Figure 3B. If Applicant would implement a redefinition of impurity concentration profile to pertain exclusively to p-type impurities (which thus far has not happened, because even the present definition allows for the statement that said impurity concentration profile results from impurities of a second conductivity type, as well as from impurities of the first conductivity type), then no such gentle peak, - or any peak for that matter, can be discerned from Figure 3B. On the other hand, Prior Art Figure 21 shows a p-type impurity concentration profile within the p-type region that is gentle (at no point is there a discontinuity of the profile itself, nor of its second order spatial derivative; please note that the p-type impurity region ends then where the n-type impurity region starts).

With regard to the "plurality of trenches formed to extend into but not through said second conductivity type region" (claim 3) (cf. comments on page 8 of said Amendment B) please be referred to Figure 11 in Huang (6,110,799) as made of record and cited in previous actions.

With regard to claims 34-42 and 51-55 under U.S.C. 102(e), in addition to the above comment on the trench extending into but not through the second conductivity type region, the issue of the buried region 35, in particular a traverse of the examiner's position that said buried region 35 may be viewed as two regions, was raised by

Applicant (page 9). However, as is evident from the typical impurity concentration profile as obtained through ion implantation (the method used by Huang; cf. column 2, lines 35-38) as given in standard text books (see, e.g., S. Wolf, Silicon Processing for the VLSI Era", Volume 2 – Process Integration, Figs. 9-10 on page 661 (Lattice Press, Sunset Beach, California, USA 1990), the impurity concentration profile by Huang does allow the splitting of the entire region 35 into the second conductivity type protrusion region and second conductivity type doped region of Applicant's claim 34. Although ion implantation does not necessarily lead to a monotonic for the entire region, it does lead to a monotonically declining profile in from a certain depth downward, i.e., in a deeper portion of the ion-implanted region, as witnessed by the said Figures 9-10.

Furthermore, the stipulation of order of steps in the processing of the device as alluded to on page 9 is immaterial to the semiconductor device, i.e., the product made, as opposed to the method of making the semiconductor device. Because the profiles of the impurity concentration in the prior art (Huang, region 35) and the invention (region 73/74) are not distinguished the allegation made in the second sentence of the final paragraph of page 9 is unsubstantiated. The property of the invention stated in the third sentence of said final paragraph is in the prior art (cf. Huang (cf. Figure 11)).

With regard to the final sentence of said paragraph the profile as shown by Figures 9-10 in Wolf, which are typical for ion-implantation, does meet the property alluded to here. With regard to the lateral impurity profile in region 35, as opposed to the vertical profile, it should be noted that the ion implantation step carried out in Huang (cf. column 2, lines 34-37) is implemented "once the trench 34 has been etched", and

therefore results in a decreased ion impurity density on the lateral extremities of region 35 as compared with the more centrally located sub-regions of region 35, because the gradual decrease of ion density results from the scattering and consequent stopping or slowing down of said ions.

With regard to the Remarks by Applicant in the third paragraph of page 10, the specific purpose of region 14 is immaterial in the claim language (claim 38 of Applicant), while said claim language is furthermore directed to a device irregardless of the use of said device. Moreover, because said region 14 abuts exclusively the semiconductor substrate 10 (cf. column 2, lines 1-2), the gate oxide layer 24 (cf. column 2, line 15) and the mask 12 (cf. column 2, line 2), region 14 is floating.

The discussion of claim 51 on pages 10-11 relies on the same consideration as made above for claim 38.

With regard to the traverse of the rejection of claims 3-5 and 30 under USC 103(a), please be referred to the comment made above concerning Figure 11, showing the second trench not to extend to the substrate but instead extend into but not through said second conductivity type region.

With regard to the traverse of the rejection of claims 6-10 and 31-32 under USC 103(a), Applicant's arguments rely on those for claim 3 discussed above.

With regard to the traverse of the rejection of claims 11-4 and 33 under USC 103(a), So et al and Huang pertain to closely related art (vertical trench MOSFET device), while the specific purpose as stated by So et al for the suppression of incidental turn-on of the parasitic bipolar transistor is an obvious advantage to any vertical trench

MOSFET device. Traverse of the combination of Huang and So et al is therefore unpersuasive. Also, the peripheral portion of the body region is 130, not 140 (cf. column 4, lines 35-40 for the definition of the body region 130 in So et al).

Traverse of the rejections of claims 35-36, 43-50 and 56-63 under USC 103(a) relies on the traverse of the corresponding independent claims 34, 38 and 51 discussed above.

In light of the above comments, the following art rejections are provided, while, in light of the standard use of the term "inner wall" as it pertains to any object as referring to the wall closest to the center of said object, Applicant is urged to delineate within the claim language itself which wall is meant by "inner wall", which would be sufficient to withdraw the still outstanding USC 112 rejection.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. ***Claims 1-50*** are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. In particular, it is not disclosed that the gate electrode portion in the trench is located "such that the insulation film is located between the inner

wall surface and the gate electrode" (fifth paragraph of claim 1, sixth paragraph of claim 3, fifth paragraph of claim 34, and seventh paragraph of claim 38).

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. ***Claim 1–2 and 29*** *are rejected* under 35 U.S.C. 102(b) as being anticipated by Prior Art as admitted in Applicants' disclosure.

With regard to claim 1: Prior Art, for instance as explicitly admitted by Applicants in their disclosure (cf. page 2 of Specification and Fig. 22B), teaches

a semiconductor substrate 1 (cf. page 2, lines 12-13) having a principal surface of a first conductivity type (n-type);

a second conductivity type region 3 having island shape (cf. page 2, line 17), formed on the principal surface of said semiconductor substrate wherein the second conductivity type region has an impurity concentration profile in a depth direction of the semiconductor substrate (see Figure 3B; cf. also page 21 lines 9-10 of the disclosure);

a highly doped first conductivity type region 4 (cf. page 2, lines 21-22) inside said second conductivity type region, wherein said impurity concentration

profile of said second conductivity type region changes gently in the depth direction of the semiconductor substrate (cf. Figure 3B) and wherein said impurity concentration profile of said second conductivity type region, resulting from impurities of a second conductivity type has a gentle peak at a depth greater than a junction depth of said first conductivity type region within said second conductivity type region, by virtue of the partial cancellation of n- and p-dopants near the interface of regions 3 and 4 (see Figure 3B) and the monotonically decreasing As and B dopant concentrations;

a trench 5 (cf. page 2, line 22) formed in the semiconductor substrate extending from a surface of said first conductivity type region so as to reach at least said second conductivity type region 3 on said first semiconductor substrate 1 (cf. Fig. 22B);

an insulation film 6 (cf. page 2, line 24) formed on an inner wall surface of said trench; and

an electrode portion made of polycrystalline silicon 7 (forming the gate electrode 8) (cf. page 2, line 26 – page 3, line 2) filling said trench with said insulation film interposed there between (cf. Fig. 22B).

In conclusion, the Prior Art as disclosed by Applicants anticipates claim 1.

With regard to claim 2: the electrode portion of claim 1 as taught by the Prior Art as disclosed by Applicants in Fig. 22B is formed to have a T-shaped cross section composed of a first part filling the trench and the second part

protruding on the principal surface of the semiconductor substrate (cf. Fig. 22B, particularly the T shape of the region with numeral 8).

With regard to claim 29: the semiconductor device as taught by Prior Art as Admitted by Applicant does have (cf. Figure 22B of disclosure) a second conductivity type semiconductor layer 12a; and a first conductivity type semiconductor layer 12 located on the second conductivity type semiconductor layer, wherein the principal surface of the first conductivity type is a surface of the semiconductor substrate.

(e) the invention was described in-
(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

3 ***Claims 34-42 and 51-55*** are rejected under 35 U.S.C. 102(e) as being anticipated by Huang (6,110,799). Huang teaches (cf. Figures 9 and 11) a semiconductor device comprising:

a first semiconductor layer 10 of a first conductivity type (n-type) (cf. column 2, lines 1-2);

a trench MOS structure formed on the first semiconductor layer (cf. abstract), wherein the trench MOS structure includes:

a second semiconductor layer 14 of second conductivity type (p-type) located on the first semiconductor layer (cf. column 2, lines 1-5);

a first trench 20 and 22 as depicted and described in Figure 3 (cf. column 2, lines 14-17) (left-most trench or right-most trench in Figure 9) and corresponding to regions 24 and 26 in Figure 9, penetrating the second semiconductor layer to (reach) the first semiconductor layer;

a first conductivity type (n-type) doped region 16 (cf. column 2, lines 6-8) located inside the second semiconductor layer and proximate to an inlet portion of the first trench, thereby a channel portion is defined on a sidewall surface of the first trench between the first conductivity type doped region and the first semiconductor layer;

an insulation film 24 (cf. column 2, line 19) located on an inner wall of the first trench;

a gate electrode 26 (cf. column 2, lines 18-26) located in the first trench such that the insulation film is located between the inner wall and the gate electrode;

a second trench 34 (cf. column 2, lines 38-43; cf. Figure 11, where said portion is indicated by the numeral 36) extending into but not through the second conductivity type region and positioned away from the first trench;

a second conductivity type protrusion region 35 (cf. column 2, lines 38-43) having a junction depth greater than the junction depth of the second semiconductor layer by virtue of its protrusion downward from said second semiconductor layer, the protrusion being positioned beneath the second trench 34; while because of the method of making of said second conductivity type protrusion region 35, i.e., ion implantation (cf. column 2, lines 34-37), region 35 is by necessity characterized by a monotonically decreasing

impurity concentration as a function of the depth of the location as measured by its distance to the trench. Region 35 can thus be divided into two abutting sub-regions that together form region 35, such that one region, henceforth called a "second conductivity type highly doped region" has an impurity concentration higher than that of the remaining region (henceforth called "protrusion region") and has a depth less than that of the junction of the protrusion region, the second conductivity type highly doped region being located beneath the second trench, and wherein the protrusion region encompasses the second conductivity type highly doped region.

Finally, Huang also teaches an upper electrode of metal 36 contacting the first conductivity type doped region of the trench MOS structure through the second trench. Therefore, Huang anticipates claim 34.

With regard to claim 37: the semiconductor device of claim 34 as taught by Huang has the property that the junction depth D1 of the second conductivity type protrusion region 34 is greater than the depth of the first trench (cf. column 3, lines 1-4).

With regard to claim 38: Huang teaches (Figure 9) a semiconductor device comprising:

a first semiconductor layer 10 of first conductivity type (n-type) (cf. column 2, lines 1-2);

a trench MOS structure formed on the first semiconductor layer (cf. abstract), comprising:

a second semiconductor layer consisting of the regions 14 to the right of the left-most first trench in Figure 9, of second conductivity type (p-type) (cf. column 2, lines 1-5);

a first trench (indicated as 20 and 22 on Figure 3 (cf. column 2, line 11) and comprising regions 24 and 26 in Figure 9; see column 2, lines 18-21) penetrating the second semiconductor layer to (reach) the first semiconductor layer;

a first conductivity type doped region 16 (n-type) (cf. column 2, lines 5-8) located inside the second semiconductor layer and proximate to an inlet portion of the first trench, wherein a channel portion is defined on a sidewall surface of the first trench between the first conductivity type doped region and the first semiconductor layer;

an insulation film 24 (cf. column 2, lines 14-17) located on an inner wall surface of the first trench;

a gate electrode 26 (cf. column 2, lines 18-26) located in the first trench such that the insulation film is located between wall surface and gate electrode;

a second conductivity type island 14 to the left of the left-most first trench in Figure 9, i.e., located on the first semiconductor layer and adjacent to the second semiconductor layer of the trench MOS structure, the second conductivity type island being isolated from the second semiconductor layer as defined within the context of this claim (by virtue of the isolation film portion 24 that separates it from 26 and the portions of 14 across it), while said second conductivity type island is being held in a floating state because in light of Figure 4 it is not only isolated from the gate through the

isolation film 24, but it is also isolated from metal 36 through the same insulation film 24 (see Figure 4); and

an upper electrode 36 (cf. column 2, lines 38-43), which contacts the first conductivity type doped region 35 of the trench MOS structure through a second trench 34 (cf. column 2, lines 38-43 and Figure 8), wherein the upper electrode is isolated from said second conductivity type island to the left of the left-most first trench.

With regard to claim 39: the trench MOS structure in the semiconductor device according to claim 38 as taught by Huang further comprises a second conductivity protrusion region 35 (cf. column 2, lines 38-43), the junction depth of which is greater than the junction depth of the second semiconductor layer (cf. column 3, lines 1-5), and wherein the protrusion region is positioned away from the first trench.

With regard to claim 40: the trench MOS structure of the semiconductor device according to claim 39 as taught by Huang further comprises a second trench 34 (cf. column 2, lines 38-43) located in the second conductivity type region and positioned away from the first trench, the protrusion region 35 being positioned beneath the second trench (see Figure 9).

With regard to claim 41: Because region 35 as taught by Huang is formed by ion implantation (cf. column 2, lines 34-37) region 35 is by necessity characterized by a monotonically decreasing impurity concentration as a function of the depth of the location as measured by its distance to the trench. Region 35 can thus be divided into two abutting sub-regions that together form region 35, such that one region, henceforth called a "second conductivity type highly doped region" has an impurity concentration

higher than that of the remaining region (henceforth called "protrusion region") and has a diffusion depth less than that of the junction of the protrusion region, the second conductivity type highly doped region being located beneath the second trench, and wherein the protrusion region encompasses the second conductivity type highly doped region.

With regard to claim 42: the junction depth of the second conductivity type protrusion region 35 in the semiconductor device of claim 39 as taught by Huang is greater than the depth of the first trench (cf. column 3, lines 1-5).

With regard to claim 51: Huang teaches (cf. Figure 9) a semiconductor device comprising:

a first semiconductor layer of first conductivity type (n-type) (cf. column 2, lines 1-2);

a second semiconductor layer 14 of second conductivity type (p-type) located on the first semiconductor layer (cf. column 2, lines 1-5);

a first trench (the one most to the left in Figure 9 and indicated by numerals 20, 22 in Figure 3 and 24/26 in Figure 9) penetrating the second semiconductor layer to (reach) the first semiconductor layer, wherein the second semiconductor layer is divided into a first portion (to the right of said first trench) and a second portion (to the left of said first trench), the second portion being isolated from the second portion by means of insulation film 24 (cf. column 2, line 15); a first doped region 16 (cf. column 2, lines 6-8) of first conductivity type inside the first portion of 14 and proximate to the opening of the first trench (namely that part of 16 that is to the right of said first trench); a second

doped region 16 (cf. column 2, lines 6-8) of first conductivity type located inside the second portion of 14 and proximate to the opening of the first trench (namely that portion of 16 that is to the left of said first trench); an insulation film 24 (cf. column 2, line 15) on an inner wall of the first trench; a gate electrode 26 (cf. column 2, lines 18-26) located in the first trench, wherein a first trench MOS structure is collectively formed with the first semiconductor layer, the first portion and first doped region, and a second trench MOS structure is collectively formed with the first semiconductor layer, the second portion and the second doped region, the material constitution being that of a UMOS structure, in which said first and second doped regions constitute the sources and the first semiconductor layer constitutes the drain, and with the first and second portions of 14 constituting the body regions of said UMOS structure; and an upper electrode 36 (cf. column 2, lines 38-43) contacting the first doped region 16 and first portion 14 of the first trench MOS structure, wherein the second doped region and the second portion of the second trench MOS structure, i.e., the one most to the left, are in an electrically floating state by virtue of the total electrical isolation of said second doped region and said second portion both polysilicon gate and metal electrodes 26 and 36, respectively.

With regard to claim 52: the trench MOS structure in the semiconductor device according to claim 51 as taught by Huang further comprises a second conductivity protrusion region 35 (cf. column 2, lines 38-43), the junction depth of which is greater than the junction depth of the second semiconductor layer (cf. column 3, lines 1-5), and wherein the protrusion region is positioned away from the first trench.

With regard to claim 53: the trench MOS structure of the semiconductor device according to claim 52 as taught by Huang further comprises a second trench 34 (cf. column 2, lines 38-43) located in the second conductivity type region and positioned away from the first trench, the protrusion region 35 being positioned beneath the second trench (see Figure 9).

With regard to claim 54: Because region 35 as taught by Huang is formed by ion implantation (cf. column 2, lines 34-37) region 35 is by necessity characterized by a monotonically decreasing impurity concentration as a function of the depth of the location as measured by its distance to the trench. Region 35 can thus be divided into two abutting sub-regions that together form region 35, such that one region, henceforth called a "second conductivity type highly doped region" has an impurity concentration higher than that of the remaining region (henceforth called "protrusion region") and has a diffusion depth less than that of the junction of the protrusion region, the second conductivity type highly doped region being located beneath the second trench, and wherein the protrusion region encompasses the second conductivity type highly doped region.

With regard to claim 55: the junction depth of the second conductivity type protrusion region 35 in the semiconductor device of claim 52 as taught by Huang is greater than the depth of the first trench (cf. column 3, lines 1-5).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. ***Claims 3 – 5 and 30*** *are rejected* under 35 U.S.C. 103(a) as being unpatentable over the Prior Art as disclosed by Applicants (cf. pages 2-3 of the Specification) in view of Huang (6,110,799).

Prior Art, for instance as explicitly admitted by Applicants in their disclosure (cf. page 2 of Specification and Fig. 22B), teaches

a semiconductor substrate 1 (cf. page 2, lines 12-13) having a principal surface of a first conductivity type (n-type);

a second conductivity type region 3 formed on the principal surface of said semiconductor substrate having island shape (cf. page 2, line 17);

a highly doped first conductivity type region 4 (cf. page 2, lines 21-22) formed inside said second conductivity type region, said first conductivity type inherently due to the introduction of impurities of the first conductivity type at high concentration;

a plurality of trenches or first trenches 5 (cf. page 2, line 22) each extending from a surface of said highly doped first conductivity type region so as

to reach at least said second conductivity type region on said first semiconductor substrate (cf. Fig. 22B), thereby defining a channel portion on a wall surface of each of said first trenches;

an insulation film 6 (cf. page 2, line 24) formed on an inner wall surface of each of the first trenches; and

an electrode portion made of polycrystalline silicon 7 (forming the gate electrode 8) (cf. page 2, line 26 – page 3, line 2) filled in each of the first trenches with said insulation film interposed there between (cf. Fig. 22B).

The Prior Art as disclosed by Applicants does not necessarily teach a plurality of second trenches and a second conductivity type protrusion region as stipulated in Applicants' claim 3.

However, for the specific purpose of protecting the gate trenches against breakdown, Huang (cf. Fig. 9) teaches a semiconductor device with trenches (cf. abstract, first sentence) comprising a plurality of first trenches with an electrode portion 26 made of polysilicon (cf. column 2, line 24) and insulation layer 24 (cf. column 2, line 15) similar to Applicants' first trenches, and also comprising a plurality of second trenches 34 (cf. Fig. 8 and column 3, line 39; see also column 2, lines 32 and 42) (the plurality of which is implied by the function of said second trenches as structures to be placed in between adjacent members of the said plurality of first trenches, said latter plurality being inclusive of the possibility of more than two first trenches) formed to extend into but not through said second conductivity type region 14 (cf. column 2, line 5) so that each of the second trenches is positioned between an adjacent pair of said first trenches in parallel

with said first trenches (cf. Fig. 11), such that a second conductivity type (P type) protrusion region 35 (cf. Fig. 9 and column 2, lines 41-42) is formed with a junction deeper than the junction of said second conductivity type region (cf. column 3, lines 1-4) and in electrical contact with the highly doped first conductivity type region 14. It is inherent in impurities in semiconductor material that they must have been introduced while, because of the election by Applicants of the device invention, as opposed to a method of making invention, the manner in which said impurities may be introduced is irrelevant to the present examination of the invention. Said protrusion region protrudes downwardly forming a junction that is deeper than a junction of said second conductivity type region (cf. column 3, lines 1-5), the protrusion being positioned beneath the second trench. *The aforementioned purpose for including the second trenches and protrusion,* namely the protection against breakdown of the trench gates, *is obviously useful in the specific case* of the plurality of first trenches admitted to be prior art by Applicants.

Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention as taught by the prior art as admitted by Applicants at the time it was made so as to include the further limitations involving the definitions of said plurality of second trenches and said second conductivity type protrusion region.

Finally, because the protrusion region 35 is formed by ion implantation (cf. column 2, lines 34-37) region 35 is by necessity characterized by a monotonically decreasing impurity concentration as a function of the depth of the location as measured by its distance to the trench. Region 35 can thus be divided into two abutting sub-regions that together form region 35, such that one region, henceforth called a

"second conductivity type highly doped region" has an impurity concentration higher than that of the remaining region (henceforth called "protrusion region") and has a depth less than that of the junction of the protrusion region, the second conductivity type highly doped region being located beneath the second trench, and wherein the protrusion region encompasses the second conductivity type highly doped region.

With regard to claim 4: the Prior Art as admitted by Applicants teaches the said electrode portion to have a T shaped cross section composed of a first part filling the trench and a second part protruding on the principal surface of the substrate (cf. Fig. 22B). Therefore, claim 4 does not distinguish over the prior art.

With regard to claim 5: although the Prior Art as admitted by Applicants do not necessarily teach the further limitation as defined by claim 5, Huang teaches an electrode 36 (cf. column 2, lines 39-43) connecting said highly doped first conductivity type region 16 (cf. Fig. 9) to said second conductivity type protrusion region 35 through said second trench, said contact being essential in aforementioned protection function of the plurality of second trenches, as explained above in the discussion of claim 3. Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention as defined by claim 3 at the time it was made so as to include the further limitation of claim 5.

With regard to claim 30: the semiconductor device as taught by Prior Art as Admitted by Applicant does have (cf. Figure 22B of disclosure) a second conductivity type semiconductor layer 12a; and a first conductivity type semiconductor layer 12

located on the second conductivity type semiconductor layer, wherein the principal surface of the first conductivity type is a surface of the semiconductor substrate.

6. ***Claims 6 – 10 and 31-32*** *are rejected* under 35 U.S.C. 103(a) as being unpatentable over Prior Art as admitted by Applicants and over Huang as applied to claim 3 above, and further in view of Yu et al (6,213,869 B1). As detailed above, claim 3 is unpatentable over Prior Art as admitted by Applicants in view of Huang.

Although neither the Prior Art as admitted by Applicants nor Huang teach the further limitation as defined by claim 6, it is known in the art as witnessed by Yu et al (cf. abstract, second sentence, and column 1, lines 7-15) that a floating body region creates a capacitor between body region and gate in MOSFET devices, resulting in a higher threshold voltage when the MOSFET is OFF than when it is ON, thus reducing steady state power dissipation. To combine this feature with the trench power MOSFET casu quo IGBT of Applicants is *obvious* because the higher withstand voltage aimed at needs to be achieved at reasonable costs with regard to power dissipation in the ON state. Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention as defined by claim 3 at the time it was made so as to include the further limitation of claim 6.

With regard to claim 7: Huang teaches a first electrode provided in one of said second trenches for electrically connecting the second conductivity type protrusion region to the highly doped first conductivity region through one of the second trenches, while the plural nature of said second trenches is implied by their positioning in between

the first trenches given the plural nature of said first trenches, comprising the case of more than two; hence Huang also teaches a second electrode provided in another one of said second trenches for electrically connecting the second conductivity type protrusion region to the highly doped first conductivity type region through the other one of said second trenches, the second electrode being disposed adjacent to the first electrode.

Although neither Prior Art as disclosed by Applicants nor Huang necessarily teach one of said adjacent pair of first and second electrodes to be in a floating state, said floating state would add the said type conductivity protrusion region to the floating body region for the well-defined *purpose* of enhancing the effect of the capacitor formed between the gate and the thus extended body region, thereby adding to the difference between the threshold voltages in the OFF, respectively ON states, and thus further improving the possibility to combine high OFF state threshold voltage with low power dissipation in the steady state operating mode of the device.

Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention defined by claim 3 at the time it was made so as to include the further limitation of claim 7.

With regard to claim 8: the second conductivity type protrusion region 35 is itself a highly doped region, and therefore can be thought of as split into two sub-regions, a first part, consisting of a highly doped region contacting said electrode 36 and disposed between said electrode and the remaining (second) part of said second type protrusion

region 35. Therefore, the further limitation of claim 8 does not distinguish over the prior art.

With regard to claim 9: in the Prior Art as admitted by Applicants (at least) one of said plurality of first trenches encloses the second conductivity type region entirely (cf. Fig. 22B). Therefore, the further limitation as defined by claim 9 does not distinguish over the prior art.

With regard to claim 10: Huang teaches the first trenches to be shallower than the second conductivity type protrusion regions (cf. column 3, lines 1-4) for the purpose of trench gate protection. Since each trench gate needs protection it would have been obvious to teach the further limitation of claim 10.

With regard to claims 31-32: the semiconductor device of either claim 6 or 7 as taught by Prior Art as Admitted by Applicant does have (cf. Figure 22B of disclosure) a second conductivity type semiconductor layer 12a; and a first conductivity type semiconductor layer 12 located on the second conductivity type semiconductor layer, wherein the principal surface of the first conductivity type is a surface of the semiconductor substrate.

7. ***Claims 11 – 14 and 33*** *are rejected* under 35 U.S.C. 103(a) as being unpatentable over Prior Art as admitted by Applicants in their disclosure (pages 2-3 and Fig. 22B) in view of So et al (5,895,951). As detailed above, Prior Art as admitted by Applicants anticipates claim 1.

Said Prior Art does not necessarily teach the further limitation as it is defined by claim 11.

However, the inclusion of a plurality of electric field alleviating regions formed by introducing impurities of the second conductivity type formed in a strip-wise shape so as to enclose a peripheral portion of said second conductivity type region has long been known in the art of trench MOSFET structures, as evidenced by So et al, who teach deep-P regions 116 (cf. column 4, line 9-11, and Fig. 2) annex doping trenches 112 *for the specific purpose* of suppressing incidental turn-on of parasitic bipolar transistor function (cf. column 3, lines 33-42). Said regions 116 surround the body region, enclosing a peripheral portion of it. Moreover, said regions are composed of a strip-wise third trench 112 (cf. column 4, line 4) and second conductivity type deep-P regions 116 in which impurities of the second conductivity type have been introduced in a strip-wise shape so as to enclose a peripheral portion of said second conductivity type region, whilst the pn junction of the electric field alleviating regions is deeper than a pn junction of aforementioned second conductivity type region (cf. column 3, lines 33-50 and Fig. 2). Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention as defined by claims 11 – 13.

With regard to claim 14: the further limitation as defined by claim 14 does not add anything to the device specifications and is merely a statement of obvious use. Vertical trench MOSFET devices such as defined by claim 11 have long been known by people of ordinary skills to be useful as gate driving power elements for controlling the conduction state between the back surface of their semiconductor substrate and their

source (first conductivity type region in the present invention and claims, usually highly doped, as is the case here (n+)) by using said electrode portion (comprising gate) as a control electrode. Therefore, the further limitation of claim 14 is moot as device limitation, and does not distinguish Applicants' invention over the prior art.

With regard to claim 33: the semiconductor device of claim 12 as essentially taught by Prior Art as Admitted by Applicant does have (cf. Figure 22B of disclosure) a second conductivity type semiconductor layer 12a; and a first conductivity type semiconductor layer 12 located on the second conductivity type semiconductor layer, wherein the principal surface of the first conductivity type is a surface of the semiconductor substrate.

8. ***Claims 35-36, 43-50, and 56-63*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang (6,110,799) in view of Prior Art as Admitted by Applicant. As detailed above, Huang anticipates claims 34, 38 and 51.

Huang does not necessarily teach the further limitations of claims 35-36, 43-50 and 56-63. However, it is understood in the art of vertical MOS devices that the drain electrode, inherently present in such devices, is a lower electrode contacting a semiconductor layer on the lower main face of the semiconductor wafer, said semiconductor layer being more highly doped and of a conductivity type that may be opposite to that of the semiconductor material with which it is in contact. See, for instance, Prior Art as Admitted by Applicant, particularly Figure 22B, in which a third semiconductor layer 12a of second conductivity type is located on a rear surface of the

first semiconductor layer 12, opposite to the second conductivity layer 13 (claims 35, 43, 45, 47, 49, 56, 58, 60 and 62), while the semiconductor device further comprises a lower electrode contacting said third semiconductor layer (claims 36, 44, 46, 48, 50, 57, 59, 61, and 63). The lower (drain) electrode is an inherent aspect of a UMOS as taught by Huang (cf. abstract), while it is understood in the art of vertical MOSFET technology that the third semiconductor layer serves to form a more highly conductive layer, smoothening the transition with the metallic-like electrode while providing a Zener diode for protection, whence the motivation to include the teaching in this regard by the Prior Art as Admitted by Applicant in the invention by Huang. The inventions can be combined readily, as nothing in Huang interferes with the provision of said third semiconductor layer and lower electrode. Success of the implementation of the combination of the inventions can therefore be reasonably expected.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JPM
April 18, 2003